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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,816	12/26/2001	Richard Slobodnik	550-299	4369

7590 06/18/2004

NIXON & VANDERHYE P.C.
1100 North Glebe Road, 8th Floor
Arlington, VA 22201

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,816	SLOBODNIK ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/4/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-04-2003
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 have been examined.

Specification

2. The abstract of the disclosure is objected to because of improper placement of "[Figure 2]" and should be removed. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 8 objected to because of the following informalities: The claim should read: "...a processor core; wherein said processor core...". Appropriate correction is required.

4. Claim 8 is objected to because of lack of line indentation according to 35 CFR 1.75(i).

5. Claims 23 and 24 are objected to because of the following informalities: These claims improperly depend on claim 1. For purpose of examination the Examiner will interpret these claims as being dependent on claim 18. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 9-11,13,14 and 18-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9 and 26:

These claims are unclear because the limitation used "at least one memory" implies one memory or more, and "synthesized and a custom memory" always implies more than one. The two are inconsistent and renders the claims indefinite. For reason of examination the Examiner is reading this to imply "synthesized or a custom memory".

Claims 10 and 27:

The term "adapted" is unclear and, therefore, renders the claim indefinite. It is not clear how the memory is adapted. Also "adapted" is not positive limitation.

Claims 11 and 14:

These claims are rejected because they depend on claim 10 and contain the same problems of indefiniteness.

Claims 28 and 31:

These claims are rejected because they depend on claim 27 and contain the same problems of indefiniteness.

Claims 13 and 30:

The claim limitation "in which of a plurality of different ways" is indefinite because it does not disclose the "different ways" a memory error is to be

reported. In addition, the limitation "in which of" is improperly used and poor grammar and also renders the claim indefinite.

Claim 18:

This claim sites the limitation "A method of testing a memory". Line 5 states "at least one memory". This is inconsistent with the preamble stating a memory and renders the claims indefinite. Therefore, line 5 should read: "said memory".

Claims 19-25,29 and 32-34:

These claims are rejected because they depend on claim 8 and contain the same problems of indefiniteness. As a result, all occurrences of "said at least one memory" should read "said memory".

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9, 13, 16, 17, 18-26, 30, 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo et al. (US-5661732) hereafter Lo.

Claims 1 and 18:

Lo teaches a ABIST micro-processor block which consists of a Micro-code Array 10, the Registers 11a-11e, and the rest of the logic known as ABIST engine 12. Lo discloses that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test

instruction). Lo also teaches the ABIST (Array Built-In Self-Test) (self-test controller) is a small programmable micro-processor used to test and characterize on-chip arrays (at least one memory). (Col. 3, lines 61-63; col. 4, lines 28-33; FIG. 1)

Claims 2 and 19:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (plurality of self-test instructions) scanned-in prior to ABIST test. (Col. 4, lines 31-33). Lo further teaches the "sequences of memory tests" from the micro-programming examples starting in column 12, line 28 and ending column 16, line 11.

Claims 3 and 20:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize (memory tests) on-chip arrays. Lo also teaches these arrays are adaptable (memory test can be changed) to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (different memories) which need to be self-tested. (Col. 3, lines 58-63).

Claims 4 and 21:

Lo teaches the programmable ABIST micro-processor block in Fig. 1 provides an improved method for testing and characterizing on-chip arrays in engineering, manufacturing, and burn-in environments (match fabrication characteristics) with programmable test patterns (different test needs), by

implementing the testing of arrays with two different logical views. (Col, 3, lines 52-56).

Claims 5 and 22:

Lo teaches of a WALKING/MARCHING pattern in FIG. 5 which shows two loops. Lo further discloses that the minor or inner loop makes sure all words (rows) have done their shift and the outer or major loop ensures that shifting has been done for all bit positions (columns). (Col. 10, lines 57-60).

Claims 6 and 23:

Lo teaches the Data Pattern Generation Logic 21 receives a 3 bit Data_ cntl code, ch_abist_data.sub_ctrl(0:2), from the Micro-Code Array's field 16 to generated various data patterns for the Array-Under-Test (self-test instruction specifies data to be written to memory). (Col. 10, lines 10-13).

Claims 7 and 24:

"...self-test controller allow one or more of the following memory test operations to be performed:

(iii) write specified data to memory locations having a checkerboard pattern of memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses"

Lo teaches of the reading and writing of a checkboard pattern with the following instructions: WO_CHKB: Initialize the whole Array With ZEROs; Load dataReg with (0101..0101); Write inverted data as address advances to form

CheckerBoard. Read CheckerBoard. Do the same with opposite data. (Col. 13, lines 7-10).

Claims 8 and 25:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize on-chip arrays (on an integrated circuit). (Col. 3, lines 61-63).

Claims 9 and 26:

Lo teaches the memory arrays are adaptable to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (synthesized and custom memory) which need to be self-tested. (Col. 3, lines 58-60).

Claims 13 and 30:

Lo teaches data read out from the memory array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation (detect memory error). (Col. 4, lines 21-25).

Claims 16 and 33:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. (Col. 4, lines 31-33).

Claims 17 and 34:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes

(self-test instruction) scanned-in (external signal pin) prior to ABIST test. (Col. 4, lines 31-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10, 11,14, 27, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732) in view of Gold (US-2003/0167428 A1).

Claims 10 and 27:

Lo does not explicitly teach "interface circuit serving to adapted values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory." Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). Gold suggests the address converter 24 (interface circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (at least one memory). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's

ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory array elements 9. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (interface circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. The artisan would have been motivated to believe so because it would enable Lo's ABIST engine 12 (self-test controller) to accommodate differing value and timing properties of a memory. The artisan also, would have been motivated to believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the memory array. In this way the interface circuit of the instant application would already be included in Gold's address converter 24 (interface circuit).

Claims 11 and 28:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (address value generated by the self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory

array elements 9. The artisan would have been motivated to do so because it would enable Lo's ABIST engine 12 (self-test controller) to access the logical addresses of the memory array elements 9.

Claims 14 and 31:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Lo does not explicitly teach of "a result data register included in the interface circuit". However, Lo does teach the data read out from the array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation. (Col. 4, lines 21-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's MISR registers to be included in Gold's memory address converter 24 (interface circuit). The artisan would have been motivated to do so because it would enable Gold's memory address converter 24 (interface circuit), already incorporated in Lo's ABIST micro-processor block, to capture the test result data.

9. Claims 12, 15, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732), hereafter Lo, in view of Correale, Jr. et al. (US-6001662), hereafter Correale.

Claims 12 and 29:

Lo does not explicitly teach the "specifying which memory to test via the self-test instruction". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different

variations of operational parameters (self-test instruction) in testing the memory array elements 9 (plurality of memories). (Col. 4, lines 46-48). Correale teaches ABIST address counter 202 is coupled to a first memory array 205, a second memory array 206 and an "Nth" memory array 208 (plurality of memories). Correale also teaches that each memory array includes a generated address mask in order to access each memory array (specifying which memory to test via the self-test instruction). (FIG. 7, Col. 6, lines 29-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 to incorporated the address masking functions of Correale's ABIST address counter 202. The artisan would have been motivated to do so because this would enable Lo to specify which to plurality of memories test.

Claims 15 and 32:

Lo does not explicitly teach the "self-test instruction specifies a size of memory to be tested". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different variations of operational parameters. (Col. 4, lines 46-48). Correale teaches an ABIST controller 92 is designed to work with a variety of different sized memory arrays (specifies a size of memory to be tested). Correale further teaches ABIST state machine 122 controls the number of iterations, the incrementing and decrementing of the addresses, when to examine array compare signals, and when to switch data patterns as well as read/write controls. Correale suggests no changes to ABIST state machine 122 are necessary to test multiple arrays of

different sizes. (Col. 6 lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 with Correale's state machine 122. The artisan would have been motivated to do so because this would enable Lo to test memories of different sizes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J. Lamarre
for

Albert DeCady
Primary Examiner

John J. Tabone, Jr.
Examiner

John J. Tabone, Jr.

Notice of References Cited	Application/Control No. 10/025,816	Applicant(s)/Patent Under Reexamination SLOBODNIK ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,661,732	08-1997	Lo et al.	714/725
	B	US-2003/0167428	09-2003	Gold, Spencer	714/720
*	C	US-6,001,662 A	12-1999	Correale et al.	438/11
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Sheet 1 of 1

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
550-299	10/025,816
APPLICANT	
SLOBODNIK et al	
FILING DATE	**GROUP**
December 28, 2001	~~2818~~ 2133

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JJ		5,535,164	7/1996	Adams et al	—	—	
JJ		5,633,877	5/1997	Shephard, III et al	—	—	
JJ		2001/0011904 A1	8/2001	Kaiser et al	—	—	
JJ		6,001,662	12/1999	Correale, Jr. et al	—	—	

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JJ		0 472 818	3/1992	EP				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, etc.)

*Examiner	John J. Tatom, Jr.	Date Considered	6/5/04

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449)